The Jitter Model for Metastability and Its Application to Redundant Synchronizers

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Abstract—**This paper has two purposes. The first is to propose and justify a new synchronizer timing model, called the jitter model, which has general application to metastable reliability analysis. The second is to apply the jitter model to show that redundancy *cannot* improve the metastable reliability of synchronizers, contradicting previous work by El-Amawy [1].**

The jitter model extends previous synchronizer input timing models by incorporating the effects of circuit noise. The circuit noise translates into jitter or random time displacement of the previously proposed *deterministic* aperture model [2]. The jitter model is supported by simulation, circuit analysis, and experimental work. An example of a CMOS *D*-type flip-flop is simulated in detail to provide a practical emphasis for the work. Also, an experimental bistable device has been constructed to examine the behavior of synchronizers with noise. Statistical results obtained from the experimental bistable support the jitter model for metastability. The model for metastability proposed by El-Amawy [1] is shown to be invalid.

The results of the original treatment of the nonviability of redundancy techniques on synchronizer metastable reliability by the author and Cantoni [2] are extended in this paper to incorporate the effects of circuit noise, contradicting work of El-Amawy [1]. This paper highlights the sensitivity of metastable reliability of redundant synchronizers to modeling assumptions.

Index Terms—**Asynchronous inputs, metastable behavior, model, noise, redundancy, synchronizer.**

I. Introduction

THE INABILITY to synchronize perfectly an asynchronous input to an independent clock is well established and is caused by the metastable behavior of basic storage elements such as flip-flops, latches, inertial delays, and Schmitt triggers [3]–[5]. The problem of metastability has not only been overlooked by some designers resulting in unreliable circuits [6], but also fundamentally misunderstood by some researchers as noted by Chaney in [7] and revealed by the discussion in [8, p. 484]. Because it is accepted that the problem of metastable failure is unavoidable [9], [3], [10], research has concentrated on methods for improving metastable reliability. The use of fast devices is successful when employed in a system implemented with slower technology [11]. However, the push for overall speed of the system dictates that other techniques also be found that are based on the same technology as the remaining logic. Redundancy is an obvious candidate because of its success in improving classical reliability where component failure is considered.

In a previous paper by the author and Cantoni [2], it was shown that redundancy and masking proved ineffectual in improving metastable reliability. This result is questioned in [1] where a different model was employed for synchronizer metastable behavior, referred to as the *El-Amawy model* in this paper. The model was claimed to incorporate the effects of circuit noise, a factor not included in the original analysis [2] which was based on a deterministic aperture model for metastability. It is shown in this current paper that the El-Amawy model is *invalid* and leads to an incorrect conclusion for the reliability analysis of redundant synchronizers. In addition, a new model for metastability is developed called the *jitter model*, which is envisaged to have general application in metastable reliability analysis.

The paper is organized as follows. A CMOS *D*-type flip-flop is introduced and analyzed in detail in Section II. Simulation results are used to obtain an input timing model incorporating the effects of noise. In Section III, a laboratory experiment is described which has been utilized to illustrate the effects of bistable noise. The results of Sections II and III form the basis for stating the jitter model of metastable behavior in synchronizers incorporating noise in Section IV. The properties of the jitter model are explored and a set of necessary and sufficient conditions are derived for an input timing model to be a jitter model. The El-Amawy model is shown not to be a jitter model. In Section V, the jitter model is applied to redundant synchronizers and their metastable reliability is compared to that of a simplex synchronizer. It is shown that redundancy cannot improve the metastable reliability of synchronizers. Thus, the jitter model and the El-Amawy model lead to contradictory statements. Since the jitter model is based on simulation, noise analysis, and laboratory measurements, while the El-Amawy model has not been justified on any grounds, one must conclude that the El-Amawy model is incorrect. The conclusions are stated in Section VI and a glossary of symbols is included.

II. Example of a Synchronizer

This section examines a CMOS *D*-type flip-flop (Fig. 1) which is commonly used as a synchronizing element. The circuit consists of two modules—the sample circuit and regenerative loop circuits. The sample circuit supplies the initial voltage on the regenerative loop which is determined by the timing relationship between clock and data inputs. The re-

Manuscript received August 14, 1987; revised July 14, 1988. This work was supported by a grant from the Australian Telecommunications and Electronic Research Board.

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IEEE Log Number 9035956.

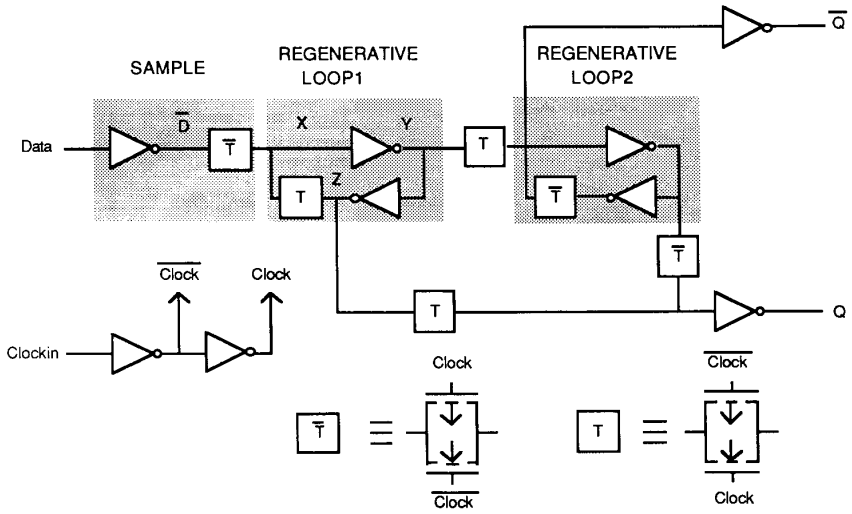


Fig. 1. CMOS *D*-type flip-flop.

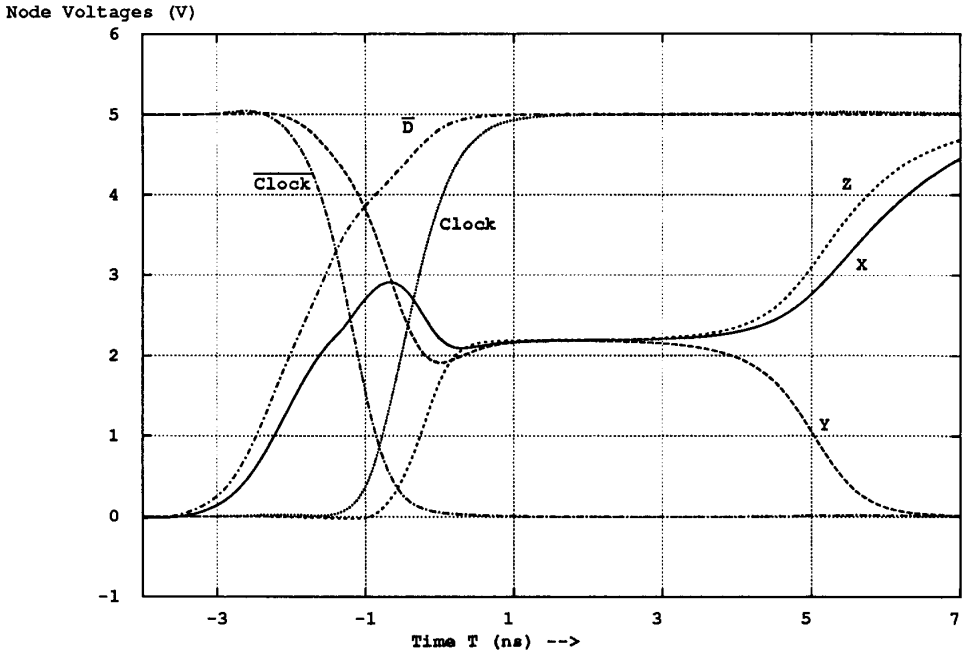


Fig. 2. SPICE simulation of CMOS *D*-type flip-flop.

generative circuit distinguishes between a 0 or 1 data value sampled. Metastable behavior occurs when the regeneration process takes an extended time to resolve to either a 0 or 1 value. The flip-flop is analyzed in Section II-A ignoring the effects of noise, and in Section II-B transistor noise contributions are included in the analysis.

A. Deterministic Analysis

The operation of the flip-flop relies on activation and coupling of the sample module and regeneration loops, by the clock opening and closing the CMOS transmission gates [12]. The T transmission gate conducts when the clock is high. When the clock is low, node X in Fig. 1 is driven by the inverted data, which determines the initial voltages on the regeneration loop 1 when the positive clock edge arrives. The results of a SPICE [13] simulation are shown in Fig. 2. For simplicity, only one of the two regenerative loops is simulated. The simulation shows metastability in the flip-flop from $T = 0$ to approximately 5 ns. The SPICE file employed in the simulation is shown in the Appendix.

Of interest is the relationship between the *data edge time* t and the behavior of the flip-flop. The sampling process and regeneration process are examined separately, and are linked by the initial regenerative loop voltages. At $T = 0$, the regenerative action is just beginning and the sample transmission gate is almost off.

The X, Y, and Z node voltages are denoted V_X, V_Y, and V_Z, respectively. It is convenient to express these voltages

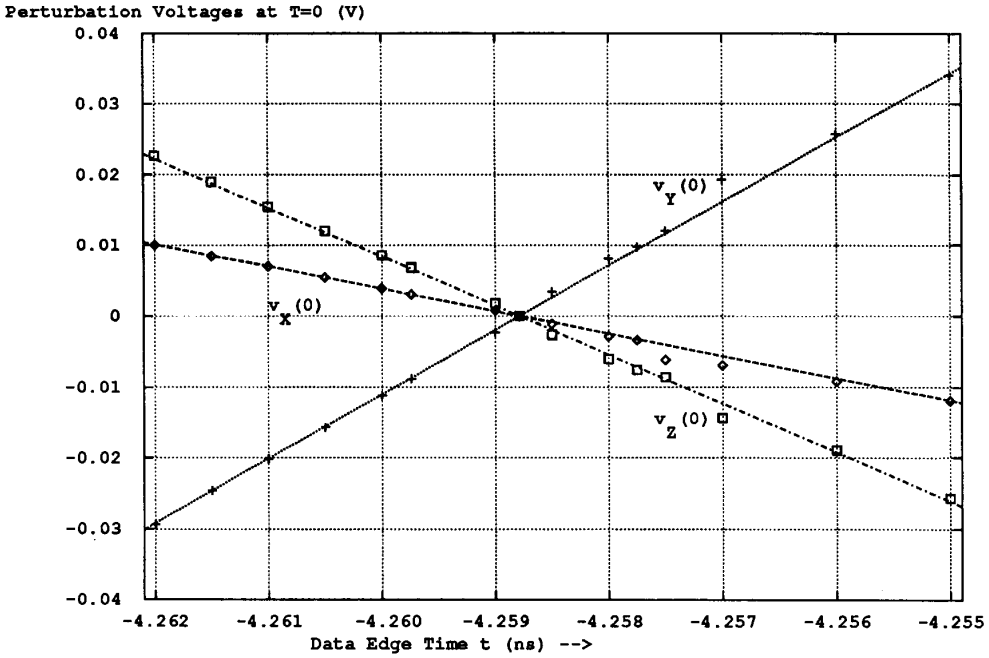


Fig. 3. Relationship between data edge time and initial regenerative loop voltages ($T = 0$).

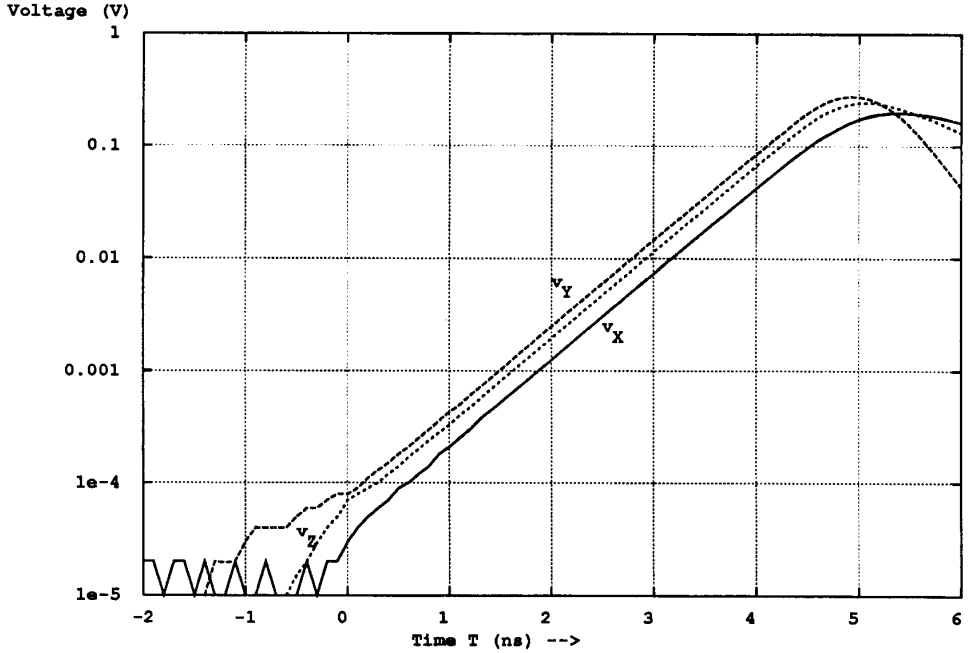


Fig. 4. Exponential regeneration of $v_X(T) = V_X(T) - V_{Xd}(T)$, $v_Y(T)$ and $v_Z(T)$. Note the onset of nonlinearity after $T = 5$.

with respect to *decision point node voltages* V_{Xd}, V_{Yd}, and V_{Zd}, which are defined to represent the zero probability trajectory of an endless metastable state, resulting from a data edge time equal to the *decision time* $t_d \cong -4.258785$ ns. *Perturbation voltages* are defined by

$$v_X(T) = V_X(T) - V_{Xd}(T). \tag{1}$$

Corresponding definitions hold for Y and Z nodes. In Fig. 3, the relationship between the voltages $v_X(0)$, $v_Y(0)$, and $v_Z(0)$ and the data edge time t is shown. The relationship is clearly linear for timing perturbations about the decision time t_d. A similar result has been reported in [14] for an nMOS flip-flop. For node Y

$$v_Y(0) = K_Y(t - t_d) \tag{2}$$

where $K_Y = 9.0614$ V/ns. The behavior of the flip-flop during regeneration is illustrated in Fig. 4. The log scale on the

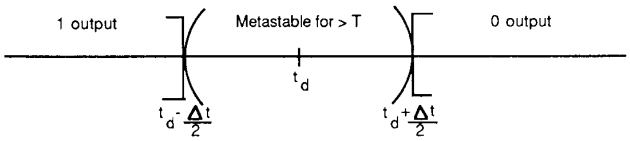


Fig. 5. Deterministic aperture model.

perturbation voltages clearly shows the exponential regeneration of the flip-flop. The time constant of regeneration τ is 0.57 ns and can be obtained from a first-order linear modeling of the bistable mechanism [15]. Thus,

$$v_Y(T) \cong v_Y(0)e^{\frac{T}{\tau}} = K_Y(t - t_d)e^{\frac{T}{\tau}}. \quad (3)$$

From the results of the simulations, a *deterministic aperture model*, as employed in [2], can be given for the sample and regeneration loop 1 of the flip-flop, as shown in Fig. 5. The model states for data edge times within $t_d - \Delta t/2$ to $t_d + \Delta t/2$ the flip-flop fails to settle from metastability within T ns. The value of Δt can be determined from (3) as follows:

$$|v_Y(T)| < v_{\text{logic}} \Leftrightarrow t_d - \Delta t/2 < t < t_d + \Delta t/2 \quad (4)$$

where $2v_{\text{logic}}$ is the voltage between the two logic states of 0 and 1, and $\Delta t = 2v_{\text{logic}}/|K_Y|e^{-\frac{T}{\tau}}$. For example, $T = 20$ ns will give an aperture width of 127×10^{-18} s.

B. Noise Analysis

The effect of MOS transistor noise on the flip-flop is analyzed in this section by considering sampling and regenerative loop processes separately. The predominant noise source in an MOS transistor is thermal noise in the channel [16], [17]. It has been erroneously suggested that shot noise plays a more dominant role [14]; however, shot noise is not present in the channel of MOS transistors because of the majority carrier conduction mechanism [16], [17].

1) Sample Noise: The sampling circuit in the example CMOS flip-flop cannot be analyzed using time invariant linear circuit techniques. The noise sources are zero mean normally distributed currents with a constant spectral density of essentially infinite bandwidth. The currents excite (finite) perturbation voltages within the circuit small enough to allow modeling by a time *varying* linear circuit, a procedure similar to that used in [14]. Consequently, the noise current $i(\nu)$ at time ν can be convolved with a time varying impulse $h(\lambda, \eta)$ to produce a voltage $v(\nu)$:

$$v(\nu) = \int_{-\infty}^{\nu} i(\lambda)h(\lambda, \eta)\,d\lambda. \quad (5)$$

The mean squared amplitude of $v(\nu)$ is equal to its variance $\text{var}[v(\nu)]$. This can be expressed in terms of the noise current autocorrelation function $R_i(\lambda, \eta)$ [18].

$$\text{var}[v(\nu)] = \int_{-\infty}^{\nu}\int_{-\infty}^{\nu} R_i(\lambda, \eta)h(\lambda, \nu)h(\eta, \nu)\,d\lambda\,d\eta. \quad (6)$$

Now the noise current's autocorrelation function for an MOS transistor [16] is a weighted impulse function given by

$$R_i(\lambda, \eta) = \frac{4}{3}kT_e|g_m|\delta(\lambda - \eta) \quad (7)$$

where k is Boltzmann's constant, T_e is the absolute temperature, g_m is the transistor's transconductance at the operating point, and δ is a unit weight impulse function. Substituting (7) into (6) gives the contribution to the noise variance from an MOS transistor.

$$\text{var}[v(\nu)] = \int_{-\infty}^{\nu} \frac{4}{3}kT_e|g_m(\lambda)|h(\lambda, \nu)^2\,d\lambda. \quad (8)$$

The impulse response function $h(\lambda, \nu)$ and transconductance $g_m(\lambda)$ are dependent on λ, the time of impulse. Due to the analytical difficulty in deriving accurate values for $h(\lambda, \nu)$ and $g_m(\lambda)$, these are obtained by simulation techniques. A pulse of current of width 0.1 ns and value 0.1 mA, approximating an impulse function with weight 10^{-14} As^{-1}, is injected into each node corresponding to the thermal noise currents, and the resulting perturbation voltages are calculated for the nodes X, Y, and Z. Examples of the impulse response functions are shown in Fig. 6 for current impulses into node X and voltages at node X. The value of g_m is calculated from the gate, source, and drain voltages of each transistor. Fig. 7 shows the noise contributions to the noise variance integrand in (8) for node Y as a function of time for each node noise source, or node pair noise source, for transmission gates. Note that the noise accumulates only after -4 ns or later due to the *decaying* impulse response during the sampling process. The largest contribution comes from node Y itself and diminishes for more distant nodes.

The rms noise voltage at $T = 0$ ns for nodes X, Y, and Z as a function of the data edge time is shown in Table I. Table I has a range of 7 ps which, somewhat surprisingly perhaps, covers a large data edge range in terms of metastable behavior. A deterministic aperture of 7 ps corresponds to a settling time of just 2 ns, or a range of 63 mV in $v_Y(0)$ which is much larger than the sampling noise standard deviation of node Y. It is clear that the noise voltages are virtually *independent* of the data edge time over a wide range. In Section II-C, this range of t will be seen to easily cover all data edge times which could result in marginal triggering of the flip-flop when noise effects from the regeneration process are included. Hence, the initial voltage on the bistable can be expressed as

$$v_Y(0) = K_Y(t - t_d) + v_{nsY} \quad (9)$$

where v_{nsY} is called *noise voltage in sampling* and is a normally distributed random variable with zero mean and standard deviation of 4.8 mV.

2) Regeneration Noise: During metastable behavior, the flip-flop can be modeled by a time *invariant* linear circuit. This is an accurate model over a limited range of voltages, outside which it will be seen in Section II-C that the probability of reentering the metastable region due to noise perturbations is extremely small. The circuit can thus be analyzed

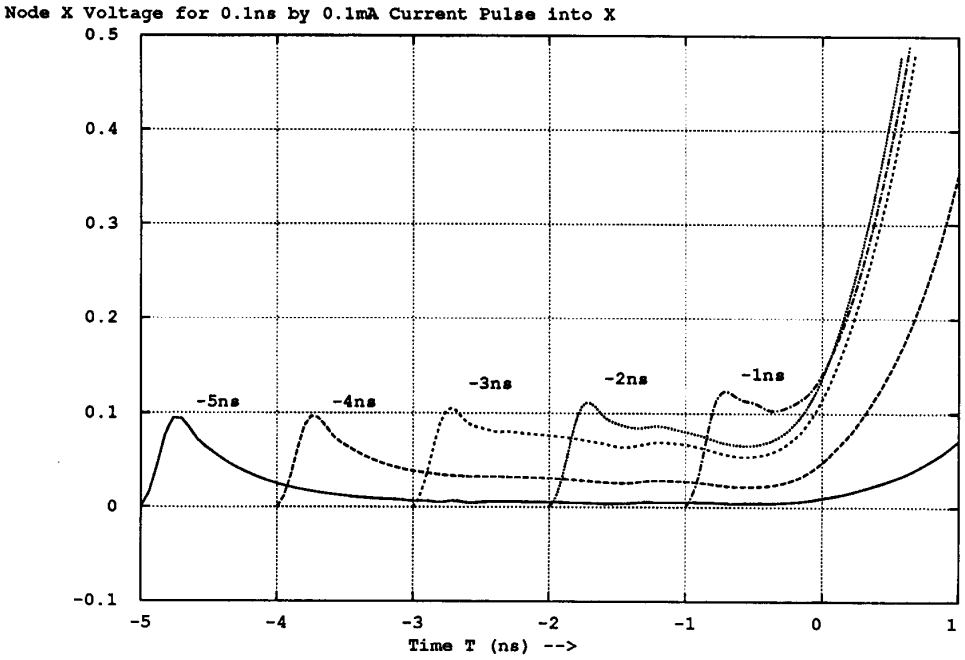


Fig. 6. Impulse response to current into node X and measured voltage at X.

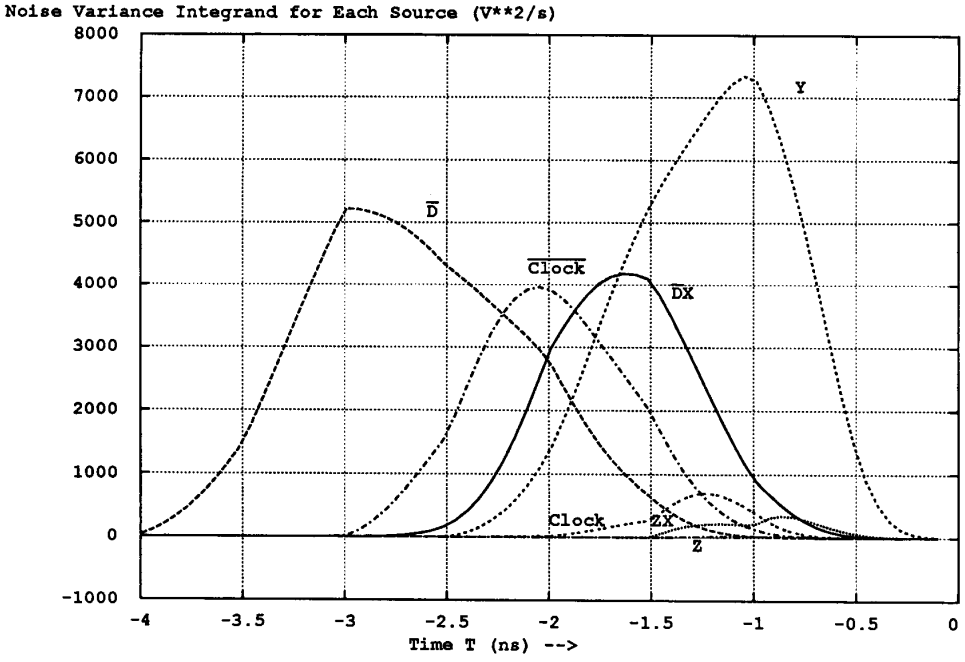


Fig. 7. Integrand of (6) as a function of time for node Y.

TABLE I
SAMPLE NOISE STANDARD DEVIATION

Data Edge Time (ns)	Standard Deviation (mV)		
	Node X	Node Y	Node Z
-4.2620	1.7256	4.8422	3.0757
-4.2615	1.7259	4.8396	3.0675
-4.2610	1.7255	4.8388	3.0645
-4.2605	1.7245	4.8387	3.0601
-4.2600	1.7214	4.8356	3.0546
-4.2590	1.7194	4.8309	3.0422
-4.2585	1.7170	4.8258	3.0347
-4.2580	1.7159	4.8314	3.0341
-4.2575	1.7126	4.8290	3.0279
-4.2550	1.7090	4.8186	3.0006

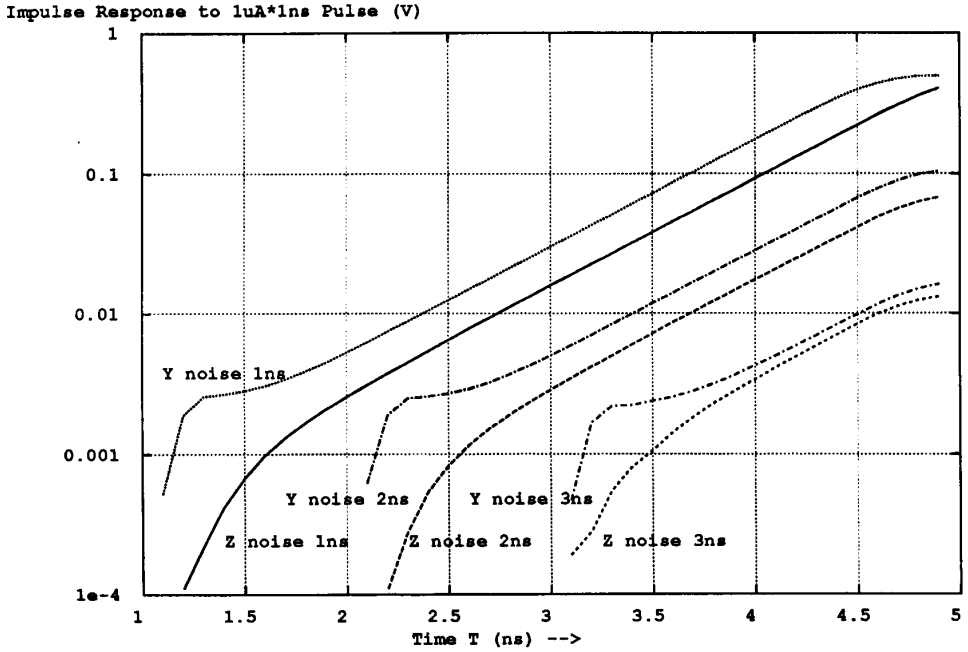


Fig. 8. Impulse responses to currents in nodes Y and Z.

by classical small signal techniques as is done in [15], [19], and [14]. The small signal analysis requires linearization of circuit models about the metastable point. It is convenient to extract the exponential impulse response directly by simulation techniques. This method also allows determination of the *range of validity* of the linear approximation.

In Fig. 8, the simulation impulse functions are shown on a logarithmic scale. A linear time invariant model for the regeneration process predicts the impulse responses to be the sum of a decaying and exploding exponential with approximately the same time constants [15], [14]. The decaying term will be insignificant after a few time constants (the order of a nanosecond). This is clearly borne out in Fig. 8 where the exploding exponential fits well 0.7 ns after the impulse. The exponential fit holds up to 5 ns which corresponds to a 1 V deviation from the decision point voltage $V_{Yd}(T)$.

The spectral densities [18] (i.e., the weighting of the impulse functions in their autocorrelation) of the noise currents generated at the nodes Y and X, and transmission gate ZX, are plotted against time for the decision point simulation in Fig. 9. Of interest is their variation as the node voltages leave the metastable region. The spectral densities remain essentially *constant* up to 5 ns or 1 V deviation from the decision point voltage. Within a ± 0.5 V range, a linear time invariant model is a good approximation.

Since the impulse response $h(\lambda, \nu)$ is independent of λ, the λ is dropped from (8). The contribution of an MOS transistor to the voltage variance is given by

$$\text{var}\,[v(T)] = \int_0^T \frac{4}{3} kT_e |g_m| |h(\nu)^2 \, d\nu. \tag{10}$$

The impulse response due to a current impulse at node i and measured at node j is denoted h_{ij}. The significant impulse functions at node Y are approximately (ignoring the decaying exponential term):

$$h_{YY}(T) = h_{YY}(0)e^{\frac{T}{\tau}}, \quad h_{ZY}(T) = h_{ZY}(0)e^{\frac{T}{\tau}}$$

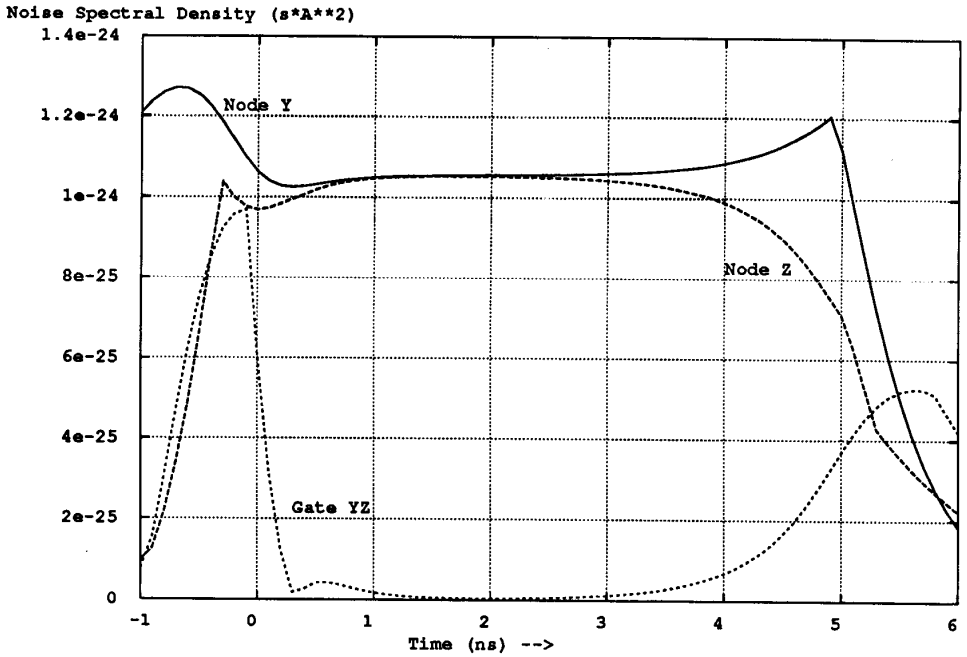


Fig. 9. Noise spectral densities during metastability.

where

$$h_{YY}(0) = 850.10^9 \text{ V/As}, \quad \text{and} \quad h_{ZY}(0) = 520.10^9 \text{ V/As}. \tag{11}$$

All other impulse responses are insignificant since their corresponding noise sources are small. Thus, from (8) the regenerative noise variance at node Y is given by

$$\text{var}[v_Y(T)] \cong \frac{4}{3}kT_e \int_0^T \left(|g_m|_Y h_{YY}^2(0) e^{\frac{2\eta}{\tau}} + |g_m|_Z h_{ZY}^2(0) e^{\frac{2\eta}{\tau}} \right) d\eta, \qquad T \gg \tau$$

$$= \frac{4}{3}kT_e \frac{\tau}{2} (|g_m|_Y h_{YY}^2(0) + |g_m|_Z h_{ZY}^2(0)) e^{\frac{2T}{\tau}} \tag{12}$$

where $|g_m|_Y$ is the sum of the absolute values of transconductance of all MOS transistors connected to node Y.

C. Input Timing Model for the Example Flip-Flop

The results of (9) and (12) are combined to give the regenerative voltage as a function of noise, data edge time t, the decision time t_d, and settling time T.

$$v_Y(T) = (K_Y(t - t_d) + v_{nsY} + v_{nrY}) e^{\frac{T}{\tau}} \tag{13}$$

where v_{nrY} is called the *noise voltage in regeneration* and is normally distributed with zero mean and variance $\frac{4}{3}kT_e\frac{\tau}{2}(|g_m|_Y h_{YY}^2(0) + |g_m|_Z h_{ZY}^2(0))$. For the example flip-flop considered above, v_{nrY} has a standard deviation of 17.3 μV which is much smaller than the 4.8 mV of v_{nsY}.

The possibility of returning to voltage zero, given that a voltage $v(T)$ has been reached, is extremely unlikely when $v(T)$ exceeds a few standard deviations of v_{nrY} as can be seen from (13). Thus, beyond a voltage as small as a millivolt one can consider the final logic state determined.

III. Experimental Verification of Regenerative Loop Noise

The behavior of the regenerative loop with transistor noise has been modeled in the laboratory by the circuit shown in Fig. 10. A bistable is formed by two operational amplifiers producing two closed loop poles at $\frac{\pm\sqrt{K_g - 1}}{RC}$, one of which is positive if the open loop gain, $K_g \cong R/R_s$, is greater than one. The open loop gain was set at approximately 10 and the time constant RC at 100 μs. The feedback is opened and closed by a JFET. Similarly, the initial voltage of the bistable is set via a JFET when the circuit's feedback loop is open. A white Gaussian noise current is applied via a JFET and a resistor when the loop is closed. The JFET's are controlled by a square wave generator with period 100 ms, which is much longer than circuit time constants. Fig. 11 shows the frequencies of low final voltages as a function of the initial voltage set on the bistable at the beginning of a sample. Each point is derived from experimental measurements on at least 10 000 samples. The fitted line is a Gaussian distribution function with standard deviation of 87.8 mV. As can be seen, a very good fit is obtained. The jitter model described in the next section is consistent with these laboratory measurements.

IV. Jitter Model for Metastability and Its Properties

A. Derivation of Jitter Model

The results of Sections II and III are generalized to produce the jitter model for metastability of synchronizers. The model

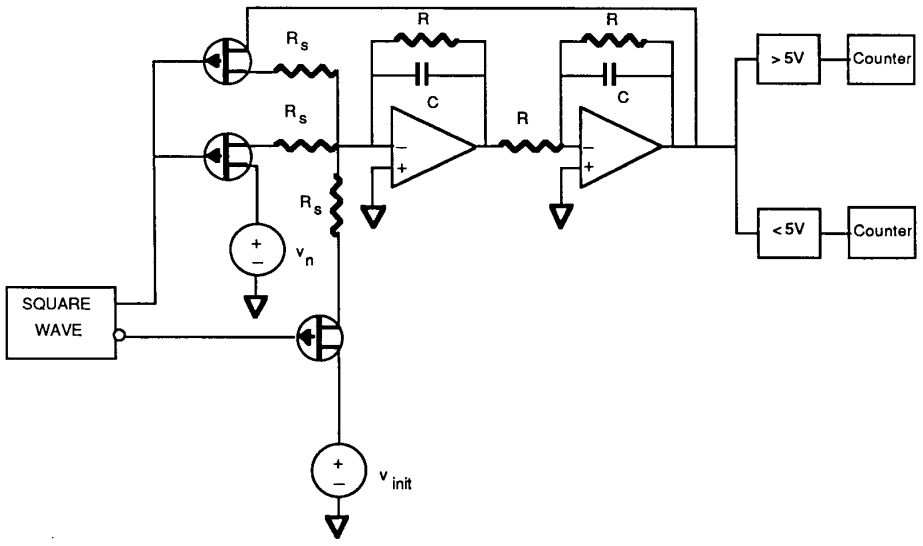


Fig. 10. Laboratory noise modeling in metastable region of synchronizer.

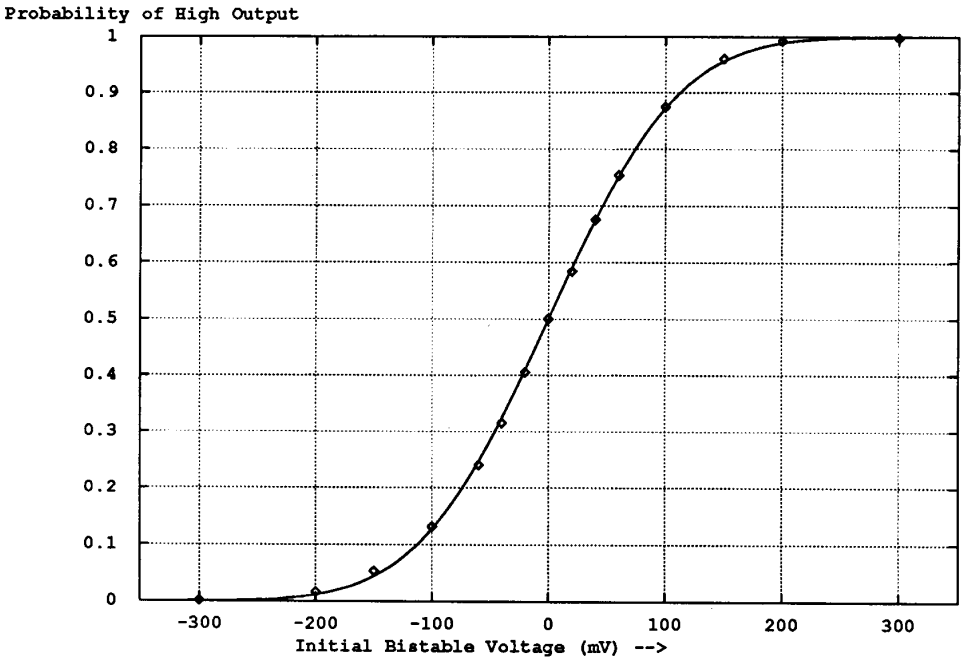


Fig. 11. Results of laboratory noise modeling in metastable region of synchronizer.

is an extension of the deterministic modeling of metastability of synchronizers known as the aperture model [2].

The synchronizer is modeled by a sample and a regeneration module as shown in Fig. 12. The sample module is assumed to generate an initial bistable voltage $v(0)$ proportional to the data edge time t, where $t = 0$ and $v(0) = 0$ correspond to the bistable unstable equilibrium state with metastability lasting indefinitely if no noise were present. Noise which is independent of t is incorporated in the sampling process.

$$v(0) = Kt + v_{ns} \tag{14}$$

where v_{ns} is a random variable with distribution that is independent of the sample time t and K is a constant. The sampling process described by (14) is linear in synchronizers (see Fig. 3) because of the short range of times and voltages over which metastability occurs. The regeneration module exponentially expands $v(0)$ and adds more noise in the process. The final bistable voltage $v(T)$ after a settling time T is assumed to be

$$v(T) = e^{\frac{T}{\tau}}[v(0) + v_{nr}] \tag{15}$$

where v_{nr} is a random variable which models the accumulated

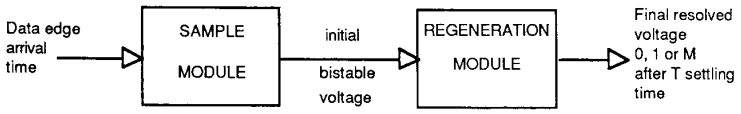


Fig. 12. General synchronizer model.

noise in the regeneration process. Substituting (14) in (15) and rearranging gives

$$t = \frac{1}{k}\left[v(T)e^{-\frac{T}{\tau}} - v_{ns} - v_{nr}\right]. \tag{16}$$

The probability of failure and resolution of the synchronizer as a function of the data edge time is dependent on the definition of the limits of the metastable region. It is assumed that resolution to either logic level is achieved when the absolute value of the bistable voltage is greater than v_{logic}. Applying (16) gives

$$\begin{aligned}&\text{prob (metastable failure)}\\ &\quad = \text{prob}\left(|v(T)| < v_{\text{logic}} \,|\, \text{data edge time of } t\right)\\ &\quad = \text{prob}\left(t \in [t_1, t_2]\right)\end{aligned} \tag{17}$$

$$\begin{aligned}&\text{prob (resolution to 1 output)}\\ &\quad = \text{prob}\left(v(T) > v_{\text{logic}} \,|\, \text{data edge time of } t\right)\\ &\quad = \text{prob}\left(t < t_1\right)\end{aligned} \tag{18}$$

$$\begin{aligned}&\text{prob (resolution to 0 output)}\\ &\quad = \text{prob}\left(v(T) < v_{\text{logic}} \,|\, \text{data edge time of } t\right)\\ &\quad = \text{prob}\left(t > t_2\right)\end{aligned} \tag{19}$$

where

$$t_1 = -\left(\frac{v_{\text{logic}}}{K}\right)e^{-\frac{T}{\tau}} + t_{\text{jitter}} \tag{20}$$

$$t_2 = +\left(\frac{v_{\text{logic}}}{K}\right)e^{-\frac{T}{\tau}} + t_{\text{jitter}} \tag{21}$$

and t_{jitter} is the sum of the random variables $-v_{ns}/K$ and $-v_{nr}/K$ and represents the time jitter due to internal synchronizer circuit noise. Although the jitter model is *not* restricted to a *Gaussian* distribution of t_{jitter}, this would normally be the case as has been demonstrated in the CMOS example.

B. Properties of the Jitter Model

Assuming the probability density function of t_{jitter} is f, the probabilities of the synchronizer resolving to 1, 0, or not at all are, respectively,

$$\text{prob}_1(t) = \text{prob}(t_1 \geq t) = \int_{t+\Delta\frac{t}{2}}^{\infty} f(\eta)\,d\eta \tag{22}$$

$$\text{prob}_0(t) = \text{prob}(t_2 \leq t) = \int_{-\infty}^{t-\Delta\frac{t}{2}} f(\eta)\,d\eta \tag{23}$$

$$\begin{aligned}\text{prob}_M(t) &= \text{prob}(t_1 < t < t_2) = \int_{t-\Delta\frac{t}{2}}^{t+\Delta\frac{t}{2}} f(\eta)\,d\eta\\ &= 1 - \text{prob}_1(t) - \text{prob}_0(t)\end{aligned} \tag{24}$$

where

$$\Delta t = t_2 - t_1 = \left(\frac{2v_{\text{logic}}}{K}\right)e^{-\frac{T}{\tau}}. \tag{25}$$

These probabilities are plotted in Fig. 13 for the CMOS example presented above for a settling time T of 20 ns and a *Gaussian* jitter time distribution. The probability functions for 0, 1, and M as a function of t that fit the jitter model are now determined. These are called *jitter probabilities*.

Definition: The functions prob_0, prob_1, prob_M are called jitter probabilities if and only if there exists a probability density function f such that (22), (23), and (24) are satisfied for some $\Delta t > 0$.

The following theorem is a direct consequence of the definition and (22), (23), and (24).

Theorem: Suppose prob_0 is a probability distribution function. The functions prob_0, prob_1, and prob_M are jitter probabilities if and only if for all t

$$\frac{d\ \text{prob}_0(t)}{dt} = -\left.\frac{d\ \text{prob}_1(u)}{du}\right|_{u=t-\Delta t}$$

$$\lim_{t\to-\infty}\text{prob}_1(t) = 1, \quad \lim_{t\to\infty}\text{prob}_1(t) = 0$$

$$0 \geq \text{prob}_1(t) \geq 1, \quad \text{prob}_M(t) = 1 - \text{prob}_1(t) - \text{prob}_0(t). \tag{26}$$

Example: The El-Amawy input timing model for metastability described in [1] can be represented as

$$\text{prob}_M(t) = \begin{cases} 0 & \text{for } t < a\\ p & \text{for } a \leq t \leq b\\ 0 & \text{for } t > b\end{cases} \tag{27}$$

$$\text{prob}_0(t) = \begin{cases} 1 & \text{for } t < a\\ \dfrac{1-p}{2} & \text{for } a \leq t \leq b\\ 0 & \text{for } t > b\end{cases} \tag{28}$$

$$\text{prob}_1(t) = \begin{cases} 0 & \text{for } t < a\\ \dfrac{1-p}{2} & \text{for } a \leq t \leq b\\ 1 & \text{for } t > b\end{cases} \tag{29}$$

where a and b are the lower and upper boundaries of the

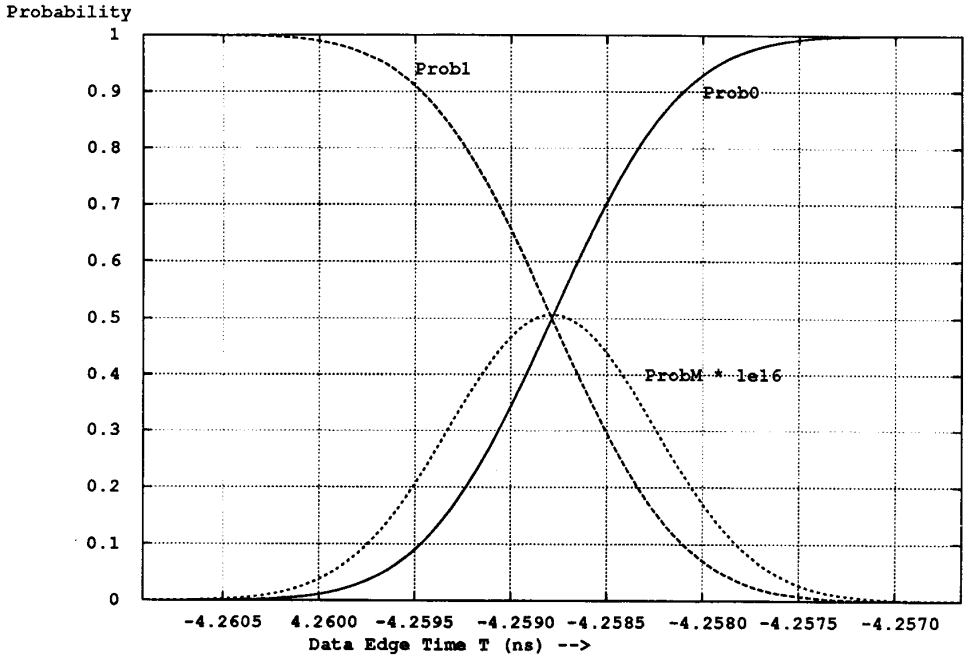


Fig. 13. Jitter model for CMOS example with settling time of 20 ns. Note that Prob_M is scaled by 10^6.

metastable aperture. It is clear that these probabilities do not conform to the jitter model described in (26). In fact, the El-Amawy model leads to an erroneous conclusion when applied to the redundant synchronizer problem as discussed below.

V. Application of the Jitter Model to Redundant Synchronizers

In a recent paper [2], it was shown that redundancy cannot improve the metastable performance of synchronizers. The input timing model, called the aperture model, was based on a noise-free model of a flip-flop. In order to study the effect of noise, a model, referred to as the El-Amawy model, was proposed [1] and is restated in (27), (28), and (29). The effect of circuit noise on the flip-flop was not analyzed in [1] but nevertheless noise was incorporated (incorrectly) with the most convenient model. When applied, the El-Amawy model predicted that redundancy *can* improve the performance of synchronizers under certain alignment conditions on the flip-flops. As shown in this paper, the El-Amawy model does not conform to the jitter model. For this reason the jitter model has been carefully tested by simulation and laboratory measurements described above. In this section, it will be shown that the jitter model supports the original conclusion of [2], namely that redundancy is ineffectual in improving metastable synchronizer performance.

A. Analysis Assumptions

The general redundant synchronizer structure considered in [2] is reproduced in Fig. 14. The design incorporates general time delays $\tau_1, \cdots, \tau_n$ for the n input flip-flops IFF1, $\cdots$, IFFn. The time delays allow relative alignment of the sampling clock edge for each flip-flop and are assumed to be much smaller than a clock period. The outputs are "voted on" with a general combinational circuit which has a constraint: if all inputs are equal, the output is equal to the inputs. The combinational circuit produces an undefined output if a metastable flip-flop is sensitized to the output as defined in [2]. The propagation delay of the combinational circuit is assumed to be zero. The assumption is a *conservative* one since a nonzero delay impairs the redundant synchronizer performance and adds further weight to this paper's conclusions. The redundant design is compared to the simplex design shown in Fig. 15. For clarity, the comparison is made under the assumption that the probability distribution of the data edge time t is uniform over a clock period. The decision time of each flip-flop is assumed to occur at the local sampling clock edge which defines $t = 0$. Variability between flip-flops is incorporated by the time delays $\tau_1, \cdots, \tau_n$. No assumptions are made concerning the distribution of the jitter times of each flip-flop except that they are independent and that the jitter time magnitude is extremely unlikely to exceed half the clock period. Metastable failure is assumed to occur when the output flip-flop, OFF, samples an undefined combinational circuit output.

B. Statement and Proof of the Ineffectuality of Redundancy

Theorem: Given the assumptions of the previous section and that the jitter model applies to the n synchronizing elements IFF1, $\cdots$, IFFn, then the probability of metastable failure of the general redundant synchronizer is as least as great as the smallest metastable failure probability of any simplex synchronizer made from one of the n synchronizing elements.

Proof: First, the probability of metastable failure of the simplex synchronizer is evaluated. Without loss of generality

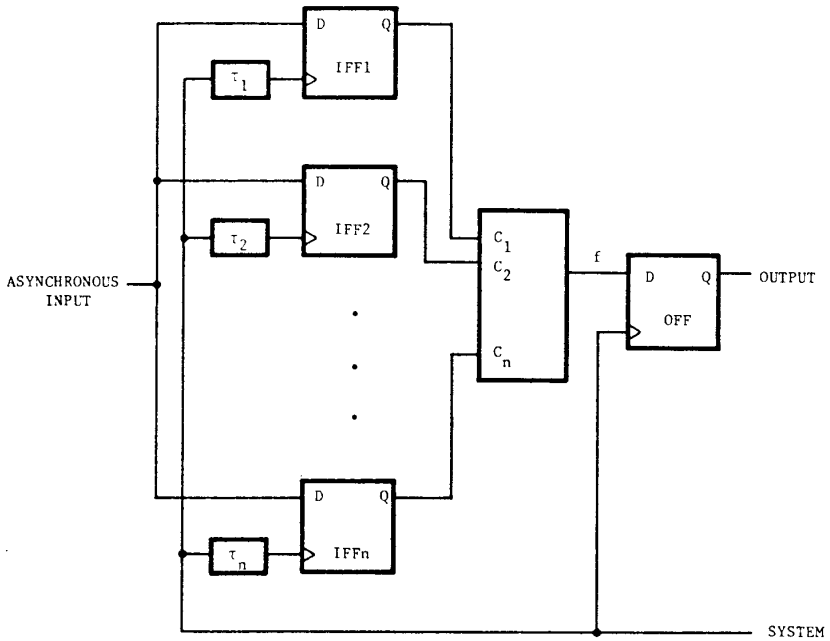


Fig. 14. General redundant synchronizer.

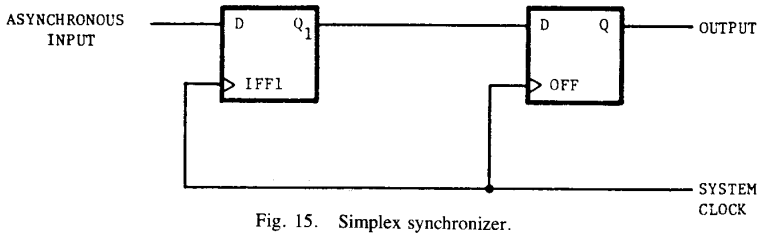


Fig. 15. Simplex synchronizer.

only a rising clock edge is considered. The *clock period* is denoted T_c. The probability of failure is dependent on both the data edge time t which is uniformly distributed between $-T_c/2$ and $+T_c/2$, and the jitter time t_j which is independently distributed with density function f. For the simplex synchronizer,

$$\begin{aligned}
&\text{prob (metastable failure)} \\
&= \int_{-T_c}^{T_c} \frac{1}{T_c} \int_{-\infty}^{\infty} f(t_j)\, \text{prob (failure}|t, t_j)\, dt\, dt_j \\
&= \frac{1}{T_c} \int_{-\infty}^{\infty} f(t_j) \int_{-T_c}^{T_c} \text{prob (failure}|t, t_j)\, dt\, dt_j \\
&= \frac{1}{T_c} \int_{-\frac{T_c}{2}-\frac{\Delta t}{2}}^{\frac{T_c}{2}-\frac{\Delta t}{2}} f(t_j) \int_{-T_c}^{T_c} \text{prob (failure}|t, t_j)\, dt\, dt_j \\
&\cong \frac{1}{T_c} \int_{-\frac{T_c}{2}+\frac{\Delta t}{2}}^{\frac{T_c}{2}-\frac{\Delta t}{2}} f(t_j)\, \Delta t\, dt_j \\
&\cong \frac{\Delta t}{T_c} \qquad (30)
\end{aligned}$$

where

$$\begin{aligned}
&\text{prob (failure}|t, t_j) \\
&= \begin{cases} 0 & \text{for } t \le t_j - \dfrac{\Delta t}{2} \\ 0 & \text{for } t \ge t_j + \dfrac{\Delta t}{2} \\ 1 & \text{for } t_j - \dfrac{\Delta t}{2} < t < t_j + \dfrac{\Delta t}{2}. \end{cases} \qquad (31)
\end{aligned}$$

The approximations in the analysis are valid when the probability of t_j being beyond the limits of a clock cycle is small. For the redundant synchronizer there are n independent jitter times $t_{j1}, \cdots, t_{jn}$ and n aperture widths $\Delta t_1, \cdots, \Delta t_n$. The decision times of the n flip-flops occur at the different times of $\tau_1, \cdots, \tau_n$ where $t = 0$ is the system sampling clock edge time. The probability of failure of the redundant synchronizer is

$$\begin{aligned}
&\text{prob (metastable failure of the redundant synchronizer)} \\
&= \int_{-T_c}^{T_c} \frac{1}{T_c} \int_{-\infty}^{\infty} f_1(t_{j1}) \cdots \int_{-\infty}^{\infty} f_n(t_{jn})
\end{aligned}$$

$$\begin{aligned}
&\text{prob}\,(\text{failure}|t, t_{j1}, \cdots, t_{jn})\, dt\, dt_{jn} \cdots dt_{j1} \\
&\quad = \frac{1}{T_c} \int_{-\infty}^{\infty} f_1(t_{j1}) \cdots \int_{-\infty}^{\infty} f_n(t_{jn}) \\
&\quad \cdot \int_{-T_c}^{T_c} \text{prob}\,(\text{failure}|t, t_{j1}, \cdots, t_{jn})\, dt\, dt_{jn} \cdots dt_{j1} \\
&\quad = \frac{1}{T_c} \int_{-\frac{T_c}{2}-\tau_1-\frac{\Delta t_1}{2}}^{\frac{T_c}{2}-\tau_1+\frac{\Delta t_1}{2}} f_1(t_{j1}) \cdots \int_{-\frac{T_c}{2}-\tau_n-\frac{\Delta t_n}{2}}^{\frac{T_c}{2}-\tau_n+\frac{\Delta t_n}{2}} f_n(t_{jn}) \\
&\quad \cdot \int_{-T_c}^{T_c} \text{prob}\,(\text{failure}|t, t_{j1}, \cdots, t_{jn})\, dt\, dt_{jn} \cdots dt_{j1}.
\end{aligned} \tag{32}$$

Given any time arrangement of the set of apertures $\Delta t_1, \cdots, \Delta t_n$ (determined by $t_{j1}, \cdots, t_{jn}$ and $\tau_1, \cdots, \tau_n$) and any combinational circuit with the properties described above it was shown in [2] that there exists t_a and t_b such that

$$\text{prob}\,(\text{failure}|t, t_{j1}, \cdots, t_{jn}) = 1 \qquad \text{for } t_a < t < t_b$$

$$\text{and} \quad t_b - t_a \geq \min\{\Delta t_i\} = \Delta t_{\min}. \tag{33}$$

Applying (33) to (32) gives

$$\text{prob}\,(\text{metastable failure of the redundant synchronizer}) \geq \frac{\Delta t_{\min}}{T_c}. \tag{34}$$

That is, the redundant synchronizer failure probability is at least as high as the best simplex synchronizer acting alone.

VI. Conclusions

This paper has developed a new model for describing metastable behavior in the presence of noise, referred to as the jitter model. Extensive simulation work and experimental measurements have been presented to support the jitter model. The model is envisaged to have wider application than the redundant synchronizer problem and to be employed in general analysis of metastable performance.

In the redundant synchronizer problem, it has been shown that the simple deterministic aperture model gives the same result as the jitter model, that is redundancy cannot improve the performance of synchronizers. This paper adds more evidence to the notion that noise has no statistical effect on metastable reliability of digital circuits as previously reported in [15], [19], and [20] where single synchronizers are considered. When multiple synchronizers sample a single input, noise has been shown, in this paper, not to effect the conclusions on any metastable reliability improvement.

Glossary of Symbols

$\|g_m\|_Y$	sum of g_m of all transistors connected to node Y.
$f(t_j)$	probability density function for jitter time t_j.
g_m	transistor transconductance.
$h(\lambda, \nu)[h(\nu)]$	voltage impulse response at time ν given a current impulse at time $\lambda[0]$.
$h_{XY}(\nu)$	$h(\nu)$ for current impulse into X, voltage measured at Y.
IFF2	input flip-flop number 2 of redundant synchronizer design.
k	Boltzmann's constant.
K_g	low frequency open loop gain of experimental bistable.
K_Y	proportionality constant in volts/second between t and initial regeneration offset voltage $v_Y(0)$, see (2).
λ, ν, η	independent time variables (as per T) used in noise analysis.
n	number of redundant synchronizers.
OFF	output flip-flop of redundant synchronizer.
$\text{prob}_1(t)\,[\text{prob}_0(t)]$	probability of resolving to 1 [0] given data edge time t.
$\text{prob}\,(\text{failure}\|t, t_j)$	probability of synchronizer failing given data edge time t and jitter time t_j.
$\text{prob}_M(t)$	probability of synchronizer *not* resolving to 1 or 0 (i.e., metastable) given data edge time t.
RC	time constant of experimental bistable.
$R_i(\lambda, \nu)$	noise current autocorrelation function, see [18].
t	data edge time.
T	independent time variable, where $T = 0$ corresponds to the onset of flip-flop regeneration.
t_1, t_2	data edge time aperture boundaries $t_1 - t_2 = \Delta t$.
t_a, t_b	$t_a < t < t_b$ guarantees failure for a set of jitter times.
Δt	time aperture width for t that results in metastable failure in the deterministic model with a settling time T.
Δt_i	Δt for flip-flop i.
$\Delta t_{\min}$	minimum Δt_i, see (33).
τ	time constant of exponential escape during regeneration.
$\tau_1, \tau_2, \cdots, \tau_n$	time delays in redundant synchronizers.
T_c	clock period of synchronizer.
T_e	absolute temperature.
$t_{j1}, \cdots, t_{jn}$	independent jitter time for n flip-flops.
t_{jitter}	random data edge time displacement.
$2v_{\text{logic}}$	minimum acceptable "1" logic voltage minus maximum acceptable "0" voltage.
v_{nrY}	noise voltage due to regeneration process, see (13).
v_{nsY}	noise voltage due to sampling process, see (9).
$V_{Xd}(T), t_d$	$V_X(T)$ for $t = -4.258785 = t_d$, known as decision point voltages because the flip-flop is exactly balanced between resolving to either 0 or 1 outputs.

$v_X(T)$ absolute node X voltage referenced to ground.

$v_X(T)$ offset between $V_X(T)$ and $V_{Xd}(T)$, see (1).

APPENDIX

SPICE FILE FOR D FLIP-FLOP

```
* Fast p-type Fast n-type
*
.OPTIONS NUMDGT=6 ITL2=300 RELTOL=0.00005 ITL4=400 ITL5=20000
* Note the value of reltot, the relative error
.MODEL NFF NMOS LEVEL=3 RSH=0 TOX=225E-10 LD=0.15E-6 XJ=0.21E-6
+ CJ=1.0E-4 CJSW=1.25E-10 UO=650 VTO=0.628 CGSO=2.3E-10
+ CGDO=2.3E-10 NSUB=3E15 THETA=0.06 KAPPA=0.4 ETA=0.14
+ VMAX=17E4 PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
.MODEL PFF PMOS LEVEL=3 RSH=0 TOX=225E-10 LD=0.4E-6 XJ=0.6E-6
+ CJ=6.0E-4 CJSW=3.75E-10 UO=220 VTO=-.668 CGSO=6.2E-10
+ CGDO=6.2E-10 TPG=-1 NSUB=5E15 ETA=0.06 THETA=0.03 KAPPA=0.4
+ VMAX=17E4 PB=0.7 MJ=0.5 MJSW=0.3 NFS=1E10
*
* deltaLpoly=0.125um deltaW=0.6um (one sided inward)
*
.SUBCKT INVERTER 1 2 3 4
* 1 input, 2 output, 3 GND, 4 Vdd
M1 2 1 3 3 NFF W=3U L=2U
M2 2 1 4 4 PFF W=3U L=2U
C1 1 3 8F
C2 2 3 50F
.ENDS
*
*
.SUBCKT TRANSGATE 1 2 3 4 5 6
* 1 input, 2 output, 3 control, 4 controlbar, 5 GND, 6 Vdd
M1 2 3 1 5 NFF W=3U L=2U
M2 2 4 1 6 PFF W=3U L=2U
R 2 5 10MEG
C1 1 5 50F
C2 2 5 50F
C3 3 5 20F
C4 4 5 20F
.ENDS
*
*
*X1 1 2 0 50 INVERTER
*X2 2 3 7 8 0 50 TRANSGATE
*X3 3 4 0 50 INVERTER
*X5 4 5 0 50 INVERTER
*X6 5 3 8 7 0 50 TRANSGATE
*X7 6 7 0 50 INVERTER
*X8 7 8 0 50 INVERTER
*
*VDD 50 0 DC 5
* VCLOCK 6 0 PULSE(5 0 0  2NS  2NS 10NS 30NS)
R1 1 0 1000
VDATA  1 0 PULSE(5 0 10.74125NS 2NS 2NS  20NS 100NS)
*Note- simulation time 0 here is equivalent T=-15ns
*IN 2 0 PULSE(0 0.1M 12NS 0 0 0.10NS 100NS)
.TRAN  0.5NS  16NS 0 .5NS
.PRINT TRAN V(1)
.WIDTH IN=75 OUT=75
.END
```

REFERENCES

[1] A. El-Amawy, "Comments on 'Can redundancy and masking improve the performance of synchronizers?'," *IEEE Trans. Comput.*, vol. 38, pp. 750–753, 1989.

[2] L. Kleeman and A. Cantoni, "Can redundancy and masking improve the performance of synchronizers?," *IEEE Trans. Comput.*, vol. C-35, no. 7, pp. 643–646, July 1986.

[3] L. R. Marino, "General theory of metastable operation," *IEEE Trans. Comput.*, vol. C-30, pp. 107–115, Feb. 1981.

[4] L. Kleeman and A. Cantoni, "Metastable behavior and digital system reliability," *IEEE Design Test Comput.*, vol. 4, no. 6, pp. 4–19, Dec. 1987.

[5] T. J. Chaney and C. E. Molnar, "Anomalous behavior of synchronizer and arbiter circuits," *IEEE Trans. Comput.*, vol. C-22, pp. 421–422, Apr. 1973.

[6] J. F. Wakerly, "The Intel MCS-48 microcomputer family: A critique," *IEEE Comput. Mag.*, vol. 22–31, Feb. 1979.

[7] T. J. Chaney, "Comments on 'A note on synchronizer and interlock maloperation'," *IEEE Trans. Comput.*, vol. C-28, pp. 802–804, Oct. 1979.

[8] W. I. Fletcher, *An Engineering Approach to Digital Design*. Englewood Cliffs, NJ: Prentice-Hall, 1980.

[9] L. Kleeman and A. Cantoni, "On the unavoidability of metastable behavior in digital systems," *IEEE Trans. Comput.*, vol. C-36, no. 1, pp. 109–112, Jan. 1987.

[10] M. Hurtado and D. L. Elliot, "Ambiguous behavior of logic bistable systems," in *Proc. 13th Annu. Allerton Conf. Circuit Syst. Theory*, Oct. 1975.

[11] G. Elineau and W. Wiesbeck, "A new J-K flip-flop for synchronizers," *IEEE Trans. Comput.*, vol. C-26, pp. 1277–1279, Dec. 1977.

[12] L. A. Glasser and D. W Dobberpuhl, *The Design and Analysis of VLSI Circuits*. Reading, MA: Addison-Wesley, 1985.

[13] A. Vladimirescu, K. Zhang, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE Version 2G User's Guide*, Berkeley, Univ. of California, 1981.

[14] J. H. Hohl, W. R. Larsen, and L. C. Schooley, "Prediction of error probabilities for integrated digital synchronizers," *IEEE J. Solid State Circuits*, vol. SC-19, pp. 236–244, Apr. 1984.

[15] H. J. M. Veendrick, "The behavior of flip-flops used as synchronizers and prediction of their failure rate," *IEEE J. Solid State Circuits*, vol. SC-24, pp. 168–176, Apr. 1980.

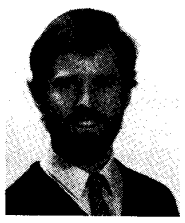
[16] R. G. Meyer and P. R. Gray, *Analysis and Design of Analog Integrated Circuits*. New York: Wiley, 1977.

[17] A. Van der Ziel, "Thermal noise in field effect transistors," *Proc. IRE*, vol. 50, pp. 1808–1812, Aug. 1962.

[18] A. Papoulis, *Probability, Random Variables, and Stochastic Processes*. New York: McGraw-Hill, 1965.

[19] G. R. Couranz and D. F. Wann, "Theoretical and experimental behavior of synchronizers operating in the metastable region," *IEEE Trans. Comput.*, vol. C-24, pp. 604–616, June 1975.

[20] D. J. Kinniment and J. F. Woods, "Synchronisation and arbitration circuits in digital systems," *Proc. IEE*, part E, vol. 123, pp. 961–966, Oct. 1976.



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